An example of the placements of the corresponding active circuit features and kerf measurement features on an integrated circuit wafer is shown in Figs. 13 and 14. Wafer 70 contains a plurality of integrated circuit areas or product cells 60 each including a plurality of active circuit features 40. Kerf areas 80, located between and adjacent to product cells 60, will eventually be cut and destroyed by the blade used to cut apart the individual product cells 60. For overlay error to be measured in the y-direction as shown, individual kerf measurement structures 40' are placed so that each of the individual features are a pre-determined distance Y from the corresponding active circuit features. For example, as shown in Fig. 14, kerf measurement feature 40' has metal line component 44' produced on the same layer as, and a distance Y in the y-direction from, active feature metal line component 44. On a different layer are kerf measurement contact hole 42' and the corresponding active circuit contact hole 42, each separated by the same distance Y. Although the kerf measurement feature 40' is shown displaced in the y direction from the corresponding active circuit feature 40, there need be no displacement in the y direction or other direction in which overlay measurement is to be determined since the kerf measurement features can be placed horizontally adjacent to the active surface features at a y distance of 0. This is shown as corresponding kerf measurement structure 40'' in Fig. 14. In each instance the kerf measurement contact hole 42', 42'' is shown displaced relative to kerf measurement metal line 44', 44'' by a distance X relative to the placement to the corresponding contact hole and metal line in active circuit feature 40.

Accordingly, the present invention provides an improved system and method for determining overlay error between different lithographically produced layers of an integrated circuit chip, particularly for determining overlay error between superimposed active circuit features on different layers of an integrated circuit chip. It overcomes the problem of discerning different superimposed active circuit features on different lithographically produced layers of an integrated circuit chip, yet does not reduce the amount of active circuit area on a semiconductor wafer. By the present invention, edges of features on different layers which are difficult to discern in active

circuit areas are readily discerned in the kerf measurement structures used for overlay error measurement.

While the present invention has been particularly described, in conjunction with a specific preferred embodiment, it is evident that many alternatives, modifications and variations will be apparent to those skilled in the art in light of the foregoing description. It is therefore contemplated that the appended claims will embrace any such alternatives, modifications and variations as falling within the true scope and spirit of the present invention.

Thus, having described the invention, what is claimed is: